CY62167E MoBL®

16-Mbit (1 M × 16 / 2 M × 8) Static RAM

Features

- Configurable as 1 M × 16 or as 2 M × 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 1.5 µA
  - Maximum standby current: 12 µA
- Ultra low active power
  - Typical active current: 2.2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Offered in 48-pin TSOP I package

Functional Description[1]

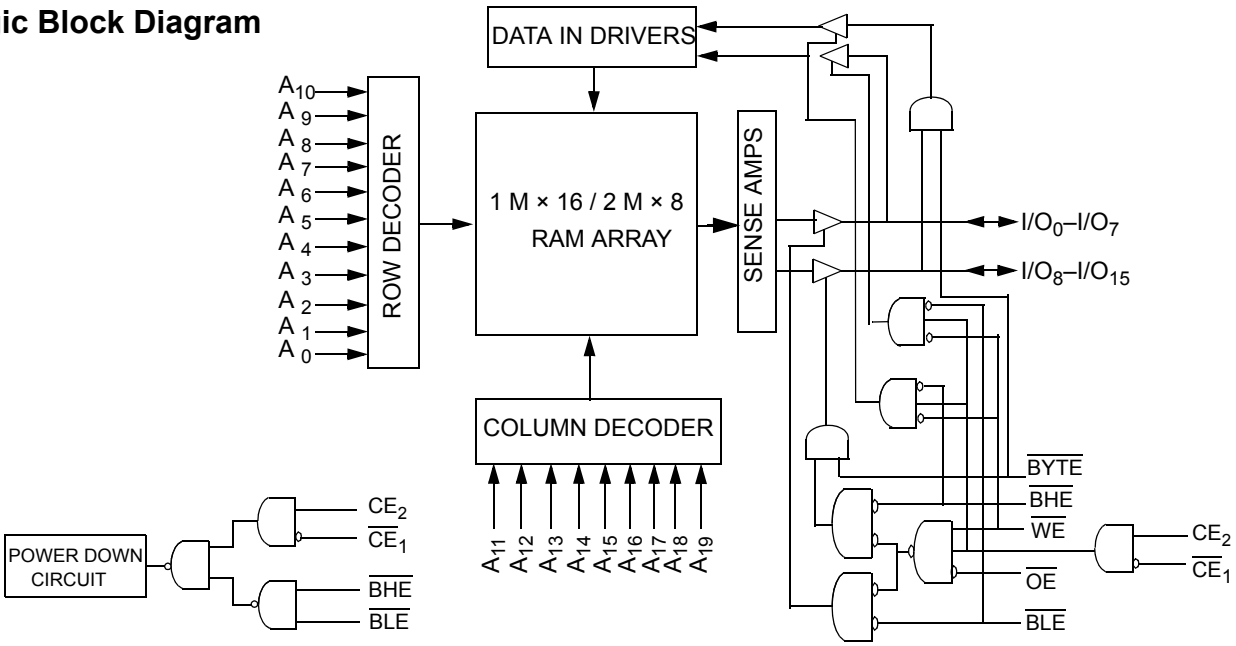
The CY62167E is a high performance CMOS static RAM organized as 1 M words by 16-bits/2 M words by 8-bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99% when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH, or CE_2 LOW, or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

- The device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both byte high enable and byte low enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or
- A write operation is in progress ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW)

To write to the device, take chip enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and write enable ($\overline{WE}$) input LOW. If byte low enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If byte high enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take chip enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If byte high enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the "Truth Table" on page 11 for a complete description of read and write modes.

Logic Block Diagram

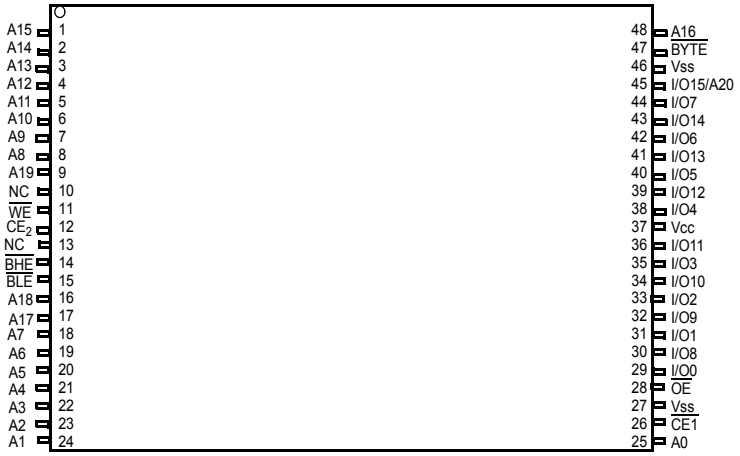


Note
1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Contents

Pin Configuration[2, 3]

48-Pin TSOP I Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[4]	Max		Typ[4]	Max	Typ[4]	Max	Typ[4]	Max
CY62167ELL	4.5	5.0	5.5	45	2.2	4.0	25	30	1.5	12

Notes
2. NC pins are not connected on the die.
3. The BYTE pin in the 48-TSOPI package must be tied to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-TSOPI package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, pin 45 is A20, while BHE, BLE and I/O_8 to I/O_{14} pins are not used.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}(typ)$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to 6.0 V

DC voltage applied to outputs in high Z state[5, 6].....–0.5 V to 6.0 V

DC input voltage[5, 6].....–0.5 V to 6.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... >2001 V (MIL-STD-883, method 3015)

Latch-up current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[7]
CY62167ELL	Industrial	–40 °C to +85 °C	4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ[9]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –1.0 mA		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 2.1 mA		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 4.5 V to 5.5 V		2.2	–	V_{CC} + 0.5 V	V
V_{IL}	Input LOW voltage	V_{CC} = 4.5 V to 5.5 V		–0.5	–	0.7[8]	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CC}(max) I_{OUT} = 0 mA CMOS levels	–	25	30	mA
		f = 1 MHz		–	2.2	4.0	mA
I_{SB2}[10]	Automatic power down current—CMOS inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, or $\overline{BHE}$ and $\overline{BLE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = V_{CC}(max)		–	1.5	12	µA

Capacitance

Parameter[11]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC}(typ)	10	pF
C_{OUT}	Output capacitance		10	pF

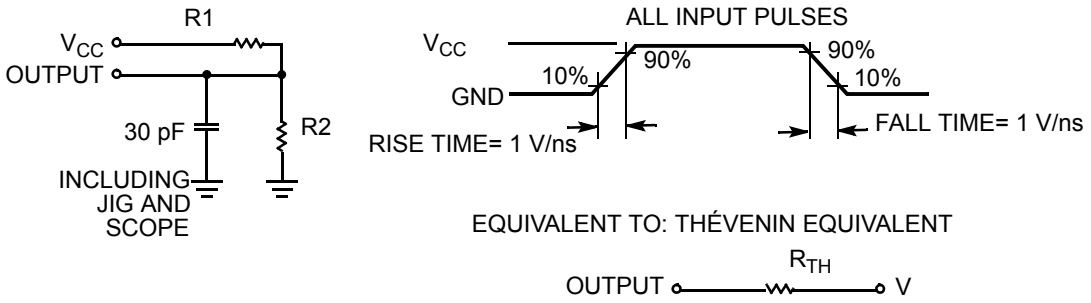
Thermal Resistance

Parameter[11]	Description	Test Conditions	TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	60	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.3	°C/W

Notes

5. V_{IL}(min) = –2.0 V for pulse durations less than 20 ns.
6. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full Device AC operation is based on a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
8. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions input LOW voltage applied to the device must not be higher than 0.7 V.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25 °C
10. Chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



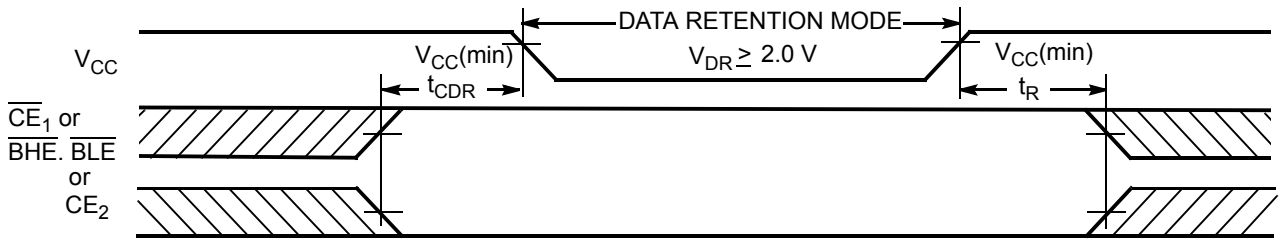
Parameters	Values	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ[12]	Max	Unit
V_{DR}	V_{CC} for data retention	–	2.0	–	–	V
I_{CCDR}[13]	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, or $\overline{BHE}$ and $\overline{BLE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	12	µA
t_{CDR}[14]	Chip deselect to data retention time	–	0	–	–	ns
t_R[15]	Operation recovery time	–	45	–	–	ns

Data Retention Waveform[16]



Notes
12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$(typ), $T_A = 25$ °C.
13. Chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 100 µs or stable at V_{CC}(min) ≥ 100 µs.
16. $\overline{BHE}$. $\overline{BLE}$ is the AND of $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter[17, 18]	Description	45 ns		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[19]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[19, 20]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low Z[19]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to high Z[19, 20]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	45	ns
t_{DBE}	BLE/BHE LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z[19]	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z[19, 20]	–	18	ns
WRITE CYCLE[21]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[19, 20]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[19]	10	–	ns

Notes

17. Test conditions for all parameters other than tristate parameters assume signal transition time of 1 V/ns, timing reference levels of V_{CC}(typ)/2, input pulse levels of 0 to V_{CC}(typ), and output loading of the specified I_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 5.
18. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 1. Read Cycle No. 1 (address transition controlled [22, 23])

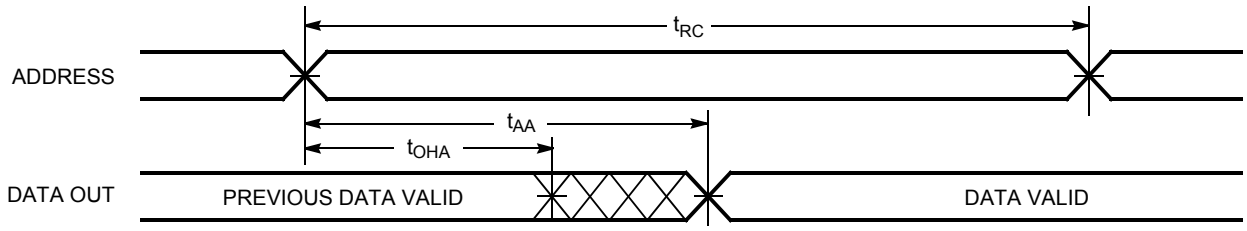
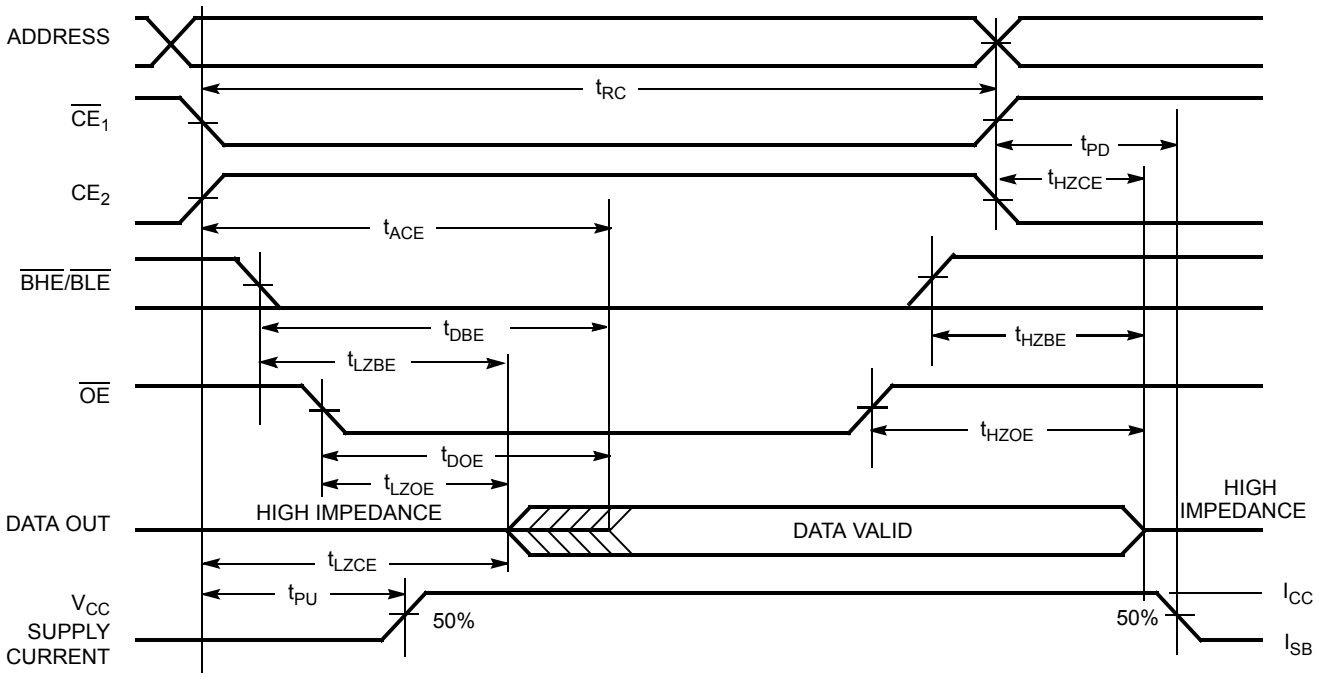


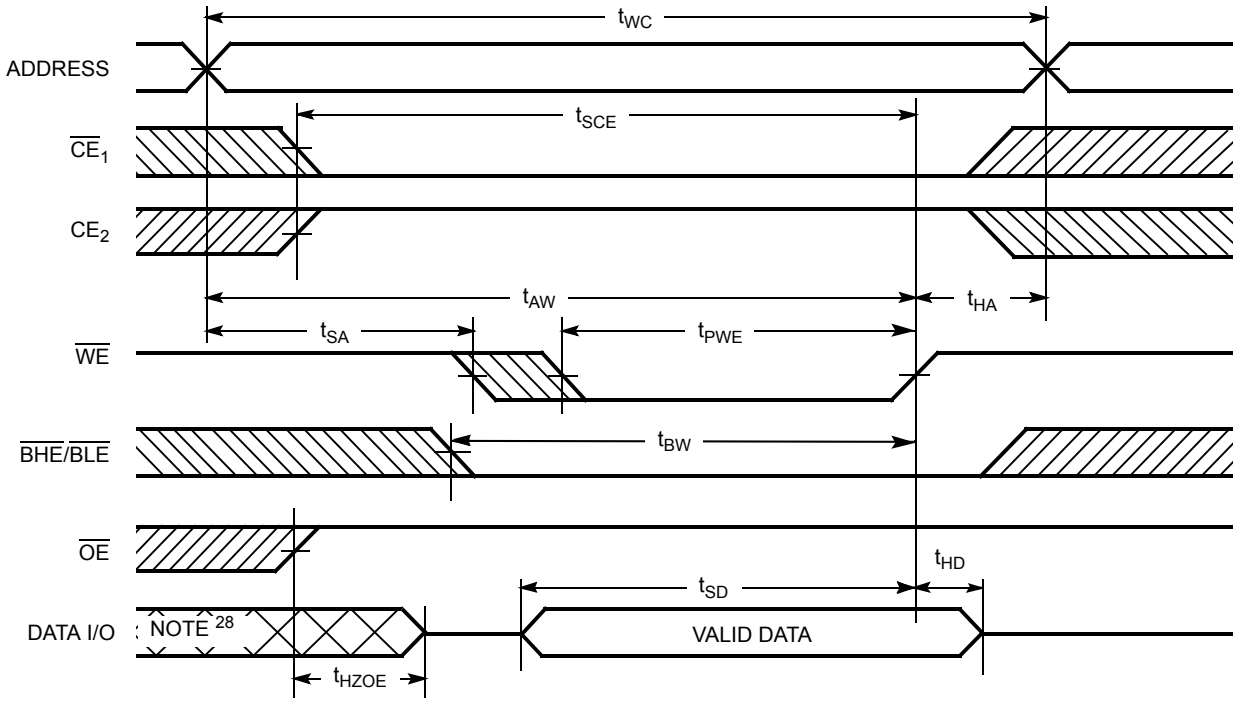
Figure 2. Read Cycle No. 2 ($\overline{OE}$ controlled [23, 24])



Notes
22. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}.
23. $\overline{WE}$ is HIGH for read cycle.
24. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms *(continued)*

Figure 3. Write Cycle No. 1 ($\overline{WE}$ controlled [25, 26, 27])



Notes

25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
28. During this period the I/Os are in output state and input signals must not be applied.

Switching Waveforms *(continued)*

Figure 4. Write Cycle No. 2 ($\overline{CE}_1$ or CE_2 controlled.[29, 30, 31])

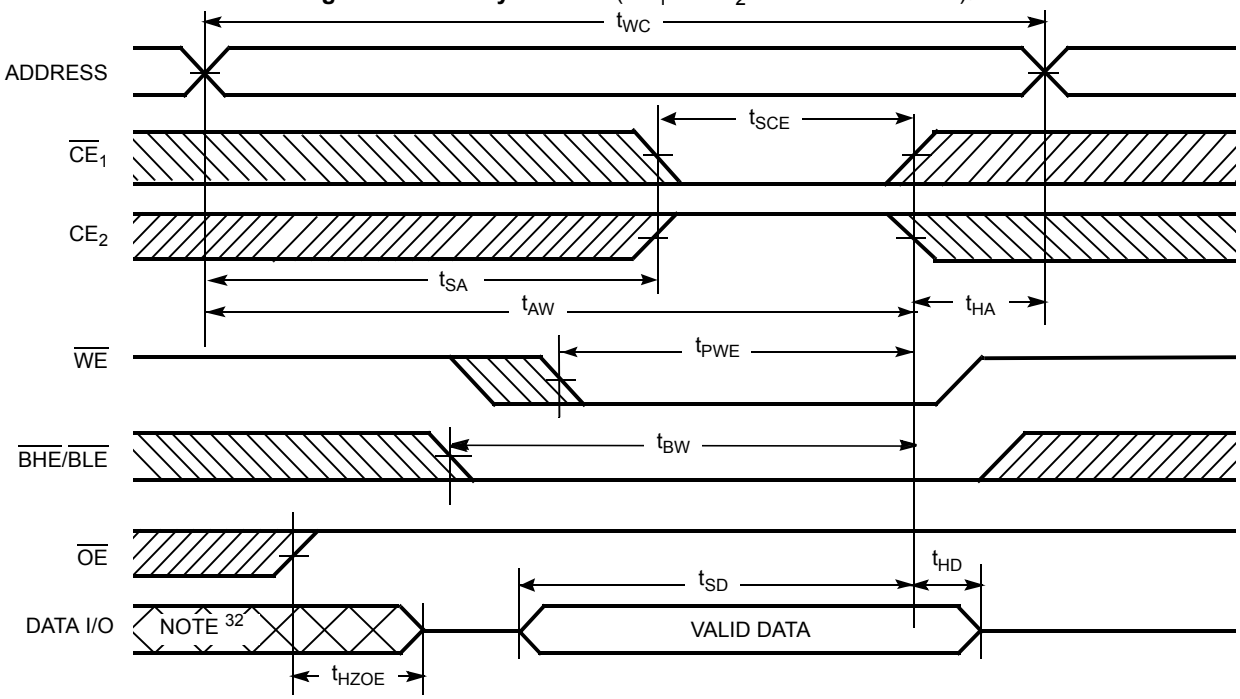
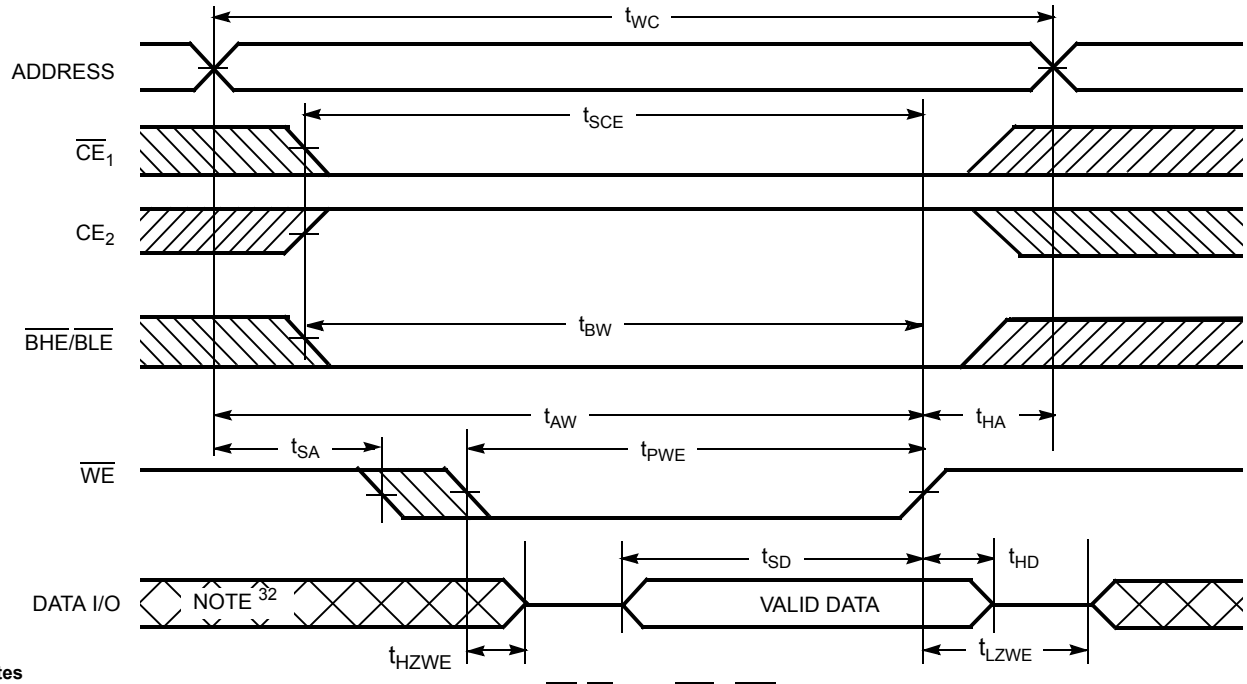


Figure 5. Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW [31])

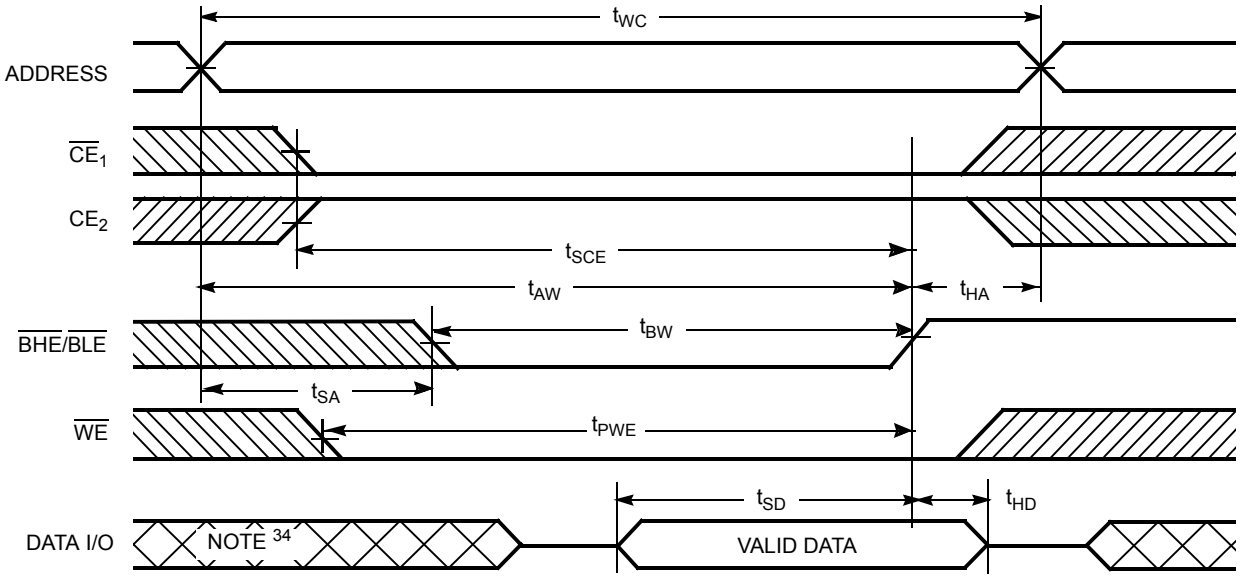


Notes

29. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
30. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
31. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
32. During this period the I/Os are in output state and input signals must not be applied.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ controlled, $\overline{OE}$ LOW [33])



Notes
33. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
34. During this period the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X[35]	X	X	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X[35]	L	X	X	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X[35]	X[35]	X	X	H	H	High Z	Deselect/power-down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data in (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data in (I/O_8–I/O_{15})	Write	Active (I_{CC})

Note
35. The 'X' (Do not care) state for the chip enables in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted

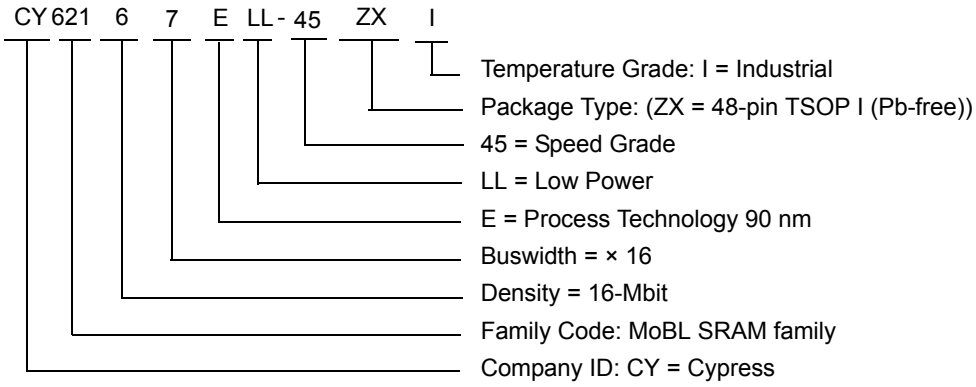
Ordering Information

Table 1 lists the CY62167ELL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key Features and Ordering Information

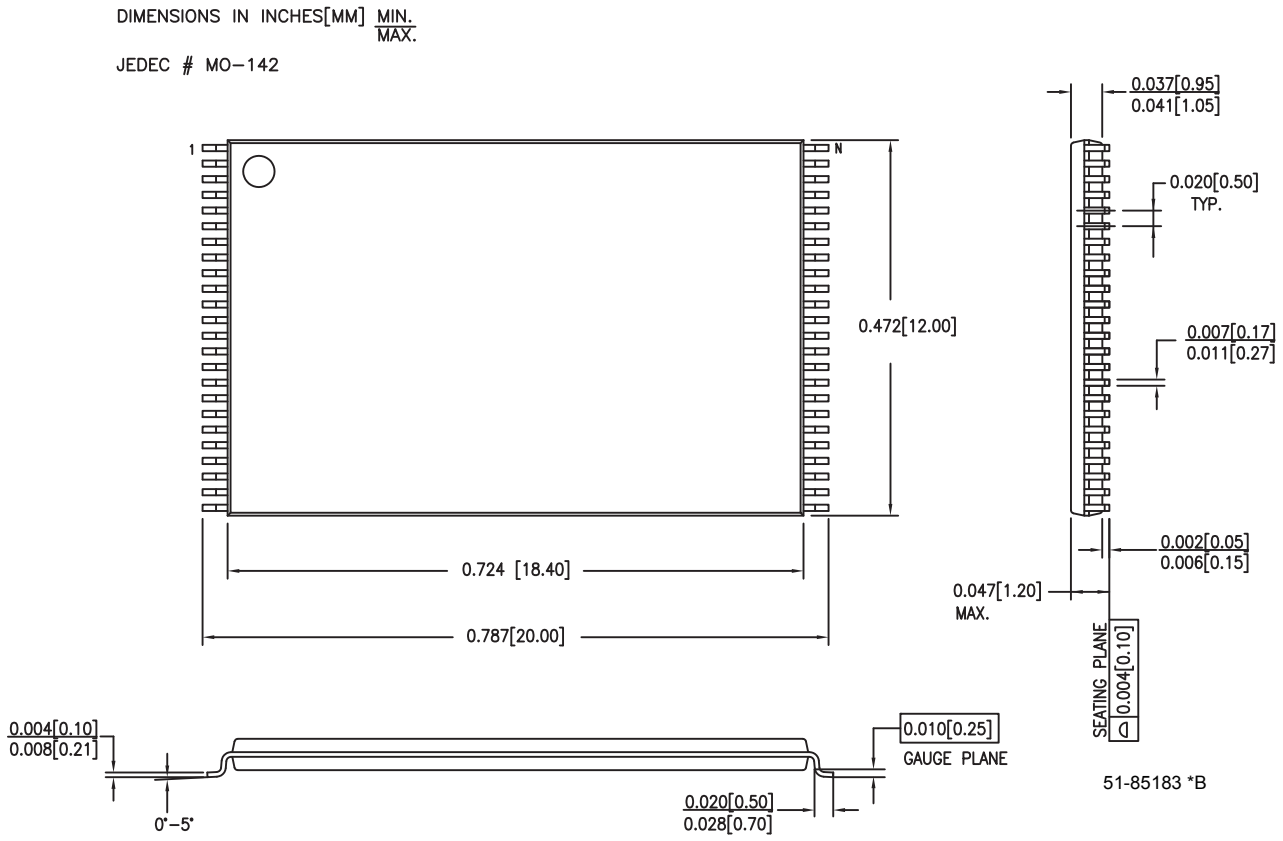
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167ELL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 7. 48-Pin TSOP I (12 mm × 18.4 mm × 1.0 mm), 51-85183



Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	volts
µA	micro amperes
mA	milli amperes
pF	pico Farad
°C	degree Celsius
W	watts

Document History Page

Document Title: CY62167E MoBL® 16-Mbit (1 M × 16 / 2 M × 8) Static RAM Document Number: 001-15607				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1103145	See ECN	VKN	New Data Sheet
*A	1138903	See ECN	VKN	Converted from preliminary to final Changed $I_{CC(max)}$ spec from 2.8 mA to 4.0 mA for f=1 MHz Changed $I_{CC(typ)}$ spec from 22 mA to 25 mA for f=f_{max} Changed $I_{CC(max)}$ spec from 25 mA to 30 mA for f=f_{max} Added footnote# 8 related to V_{IL} Changed I_{CCDR} spec from 10 µA to 12 µA Added footnote# 14 related to AC timing parameters
*B	2934385	06/03/10	VKN	Included $\overline{BHE}$, $\overline{BLE}$ in I_{SB2}, I_{CCDR} test conditions to reflect byte power down feature Added footnote #35 related to chip enable Updated package diagram Updated template

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